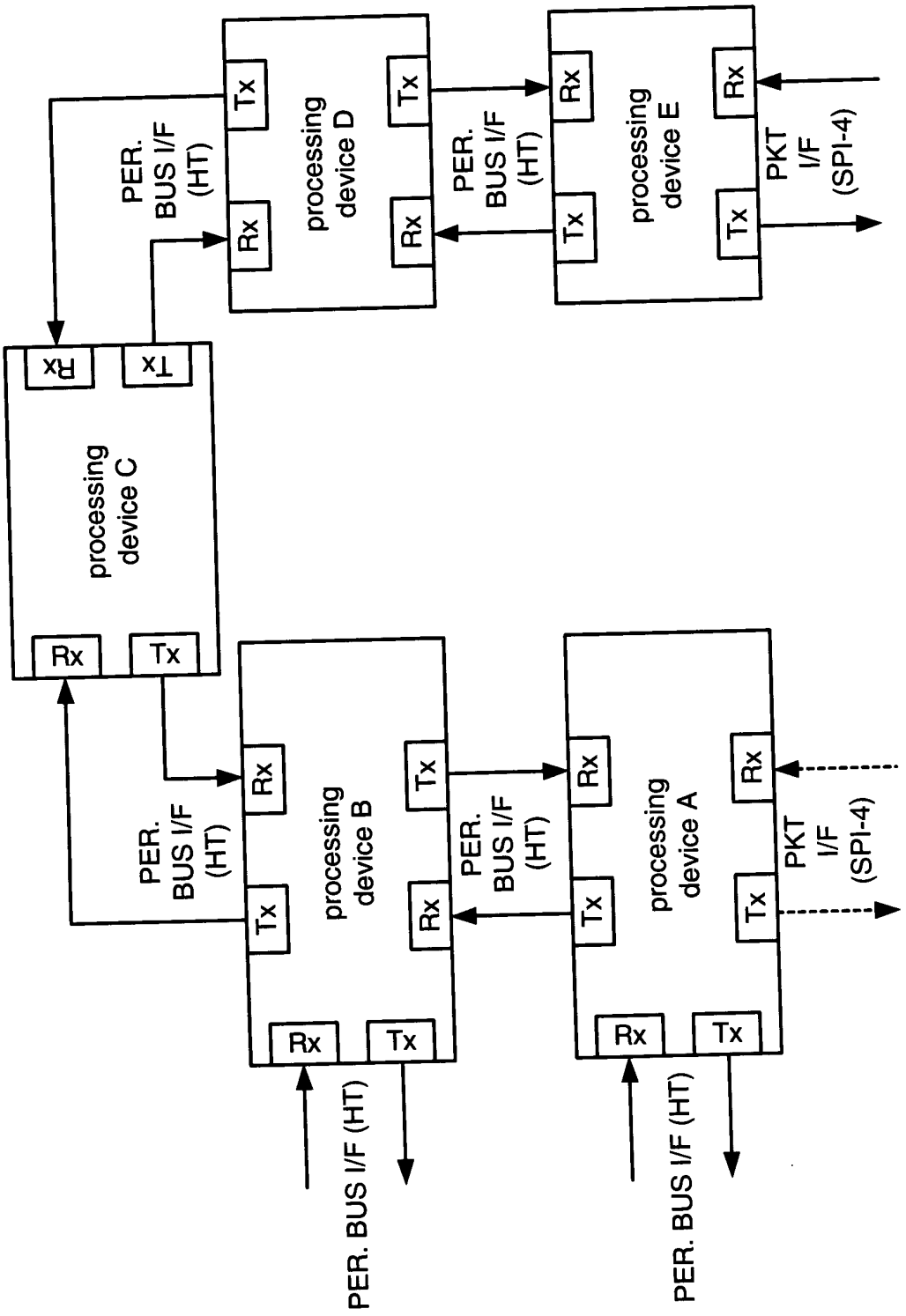


FIG. 1

proc ssing syst m 10

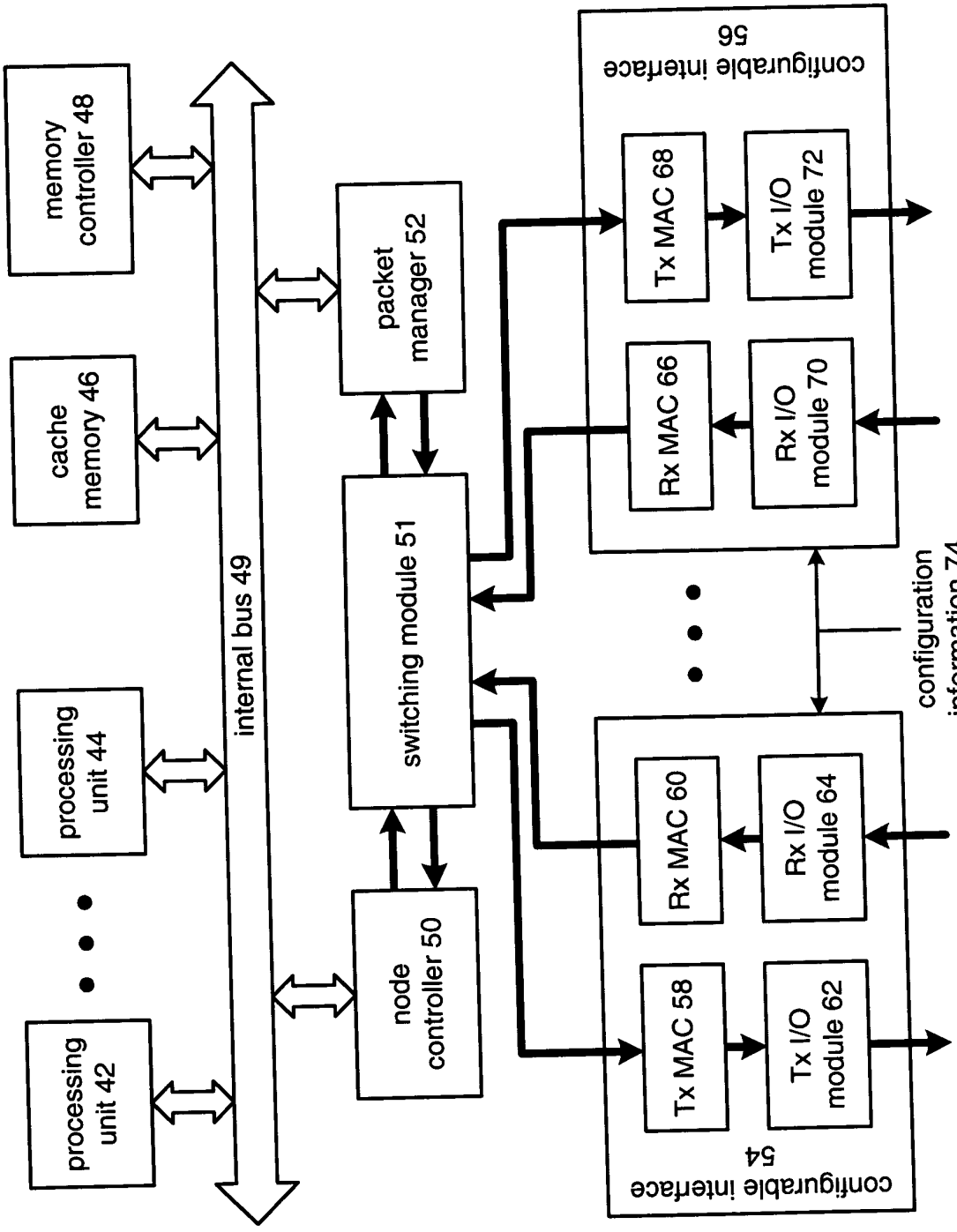


FIG. 2

processing device 20

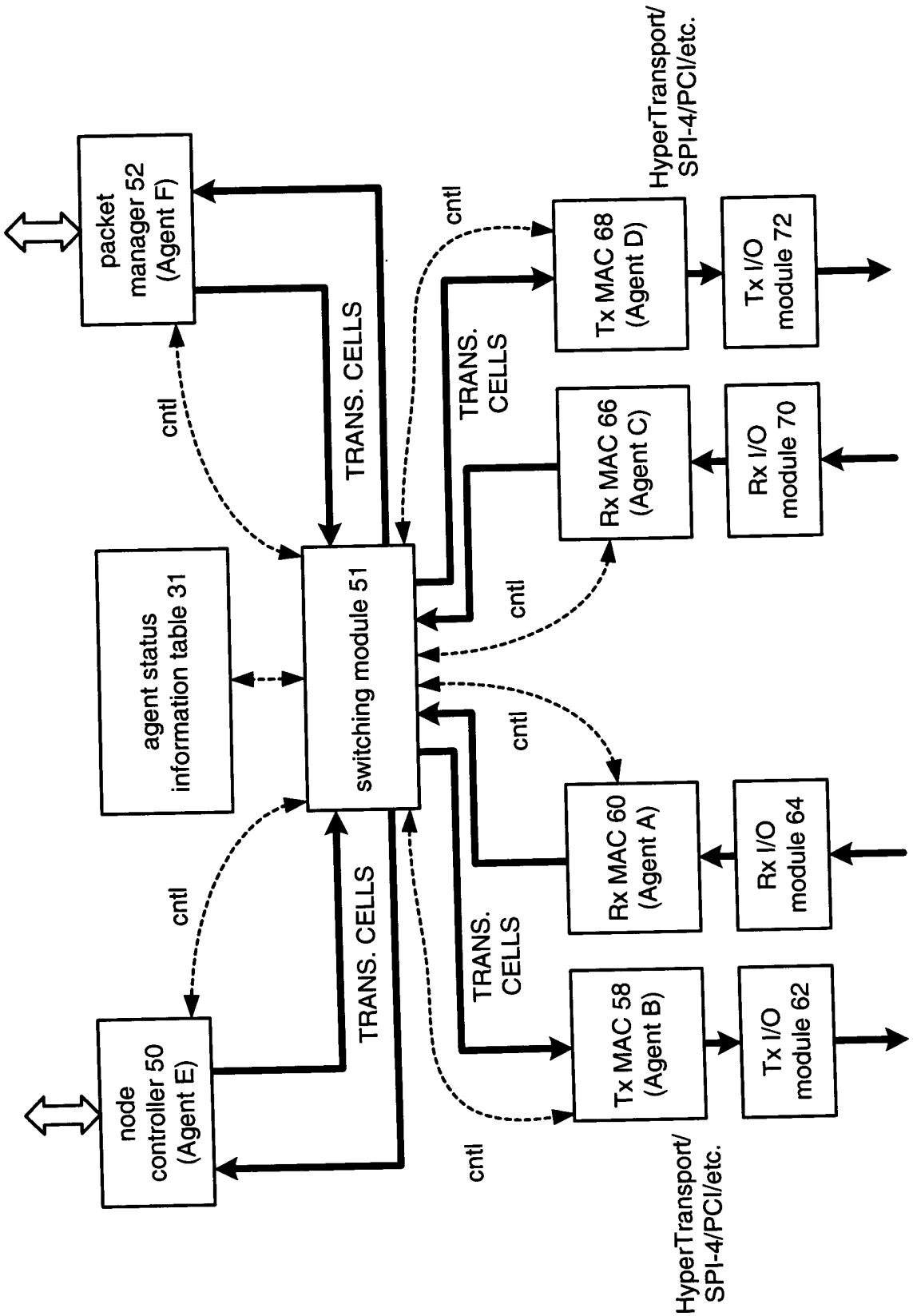
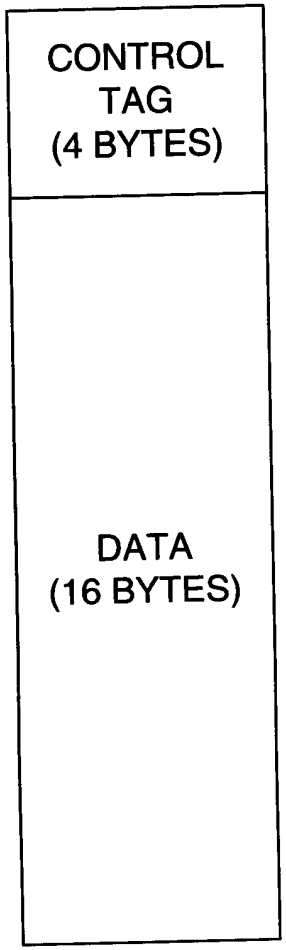


FIG. 3

processing devic 20



Transaction Cell

FIG. 4A

SRC_AGT_A STATUS	DST_AGT_B STATUS	EOP_ST
SRC_AGT_A STATUS	DST_AGT_D STATUS	EOP_ST
SRC_AGT_A STATUS	DST_AGT_E STATUS	EOP_ST
SRC_AGT_A STATUS	DST_AGT_F STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_B STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_D STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_E STATUS	EOP_ST
SRC_AGT_C STATUS	DST_AGT_F STATUS	EOP_ST
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
•	•	•
SRC_AGT_F STATUS	DST_AGT_B STATUS	EOP_ST
SRC_AGT_F STATUS	DST_AGT_D STATUS	EOP_ST
SRC_AGT_F STATUS	DST_AGT_E STATUS	EOP_ST

Agent Status Information Table

FIG. 4B

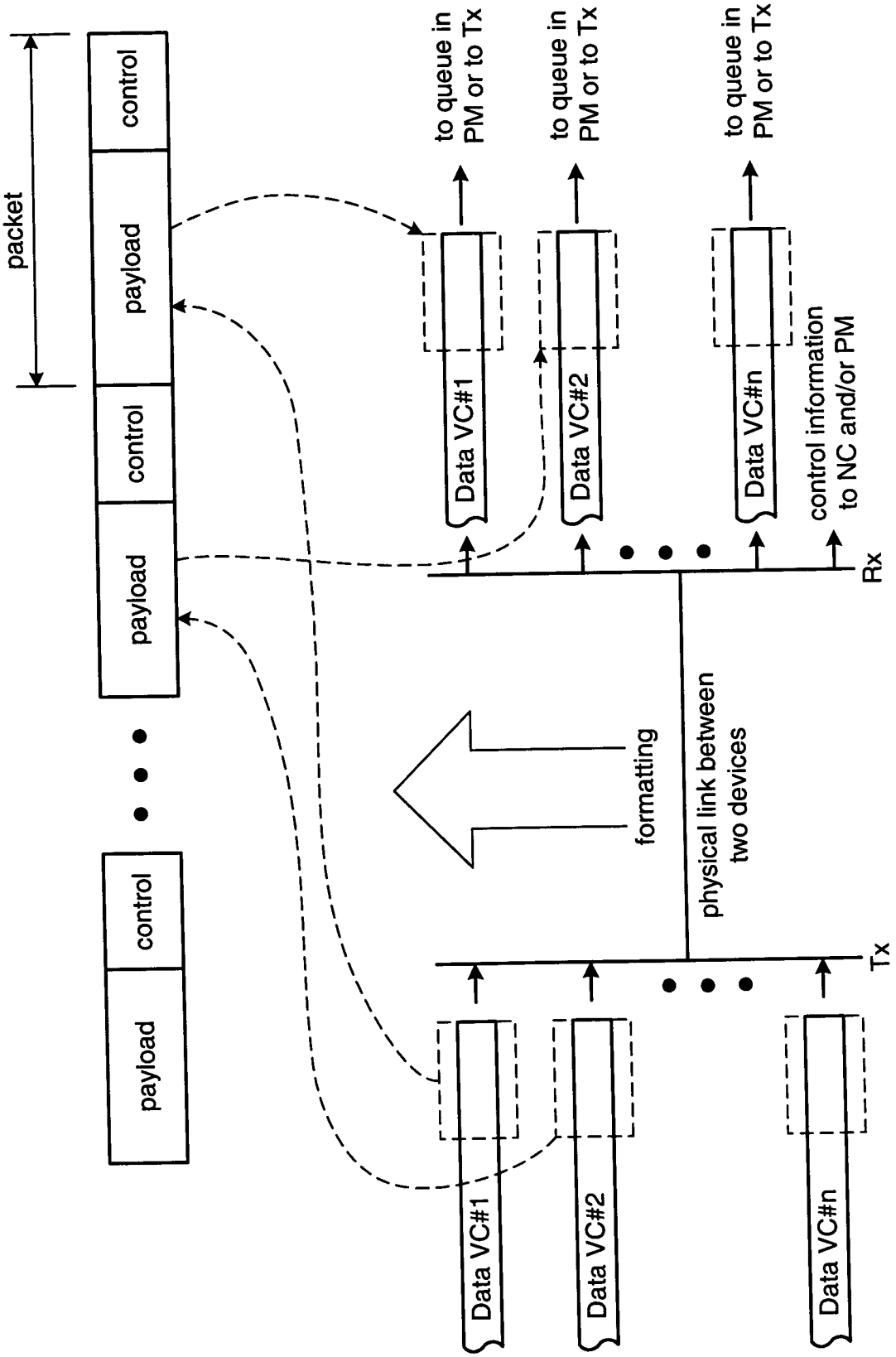


FIG. 5
data mapping for I/O modules 62, 64, 70, and/or 72

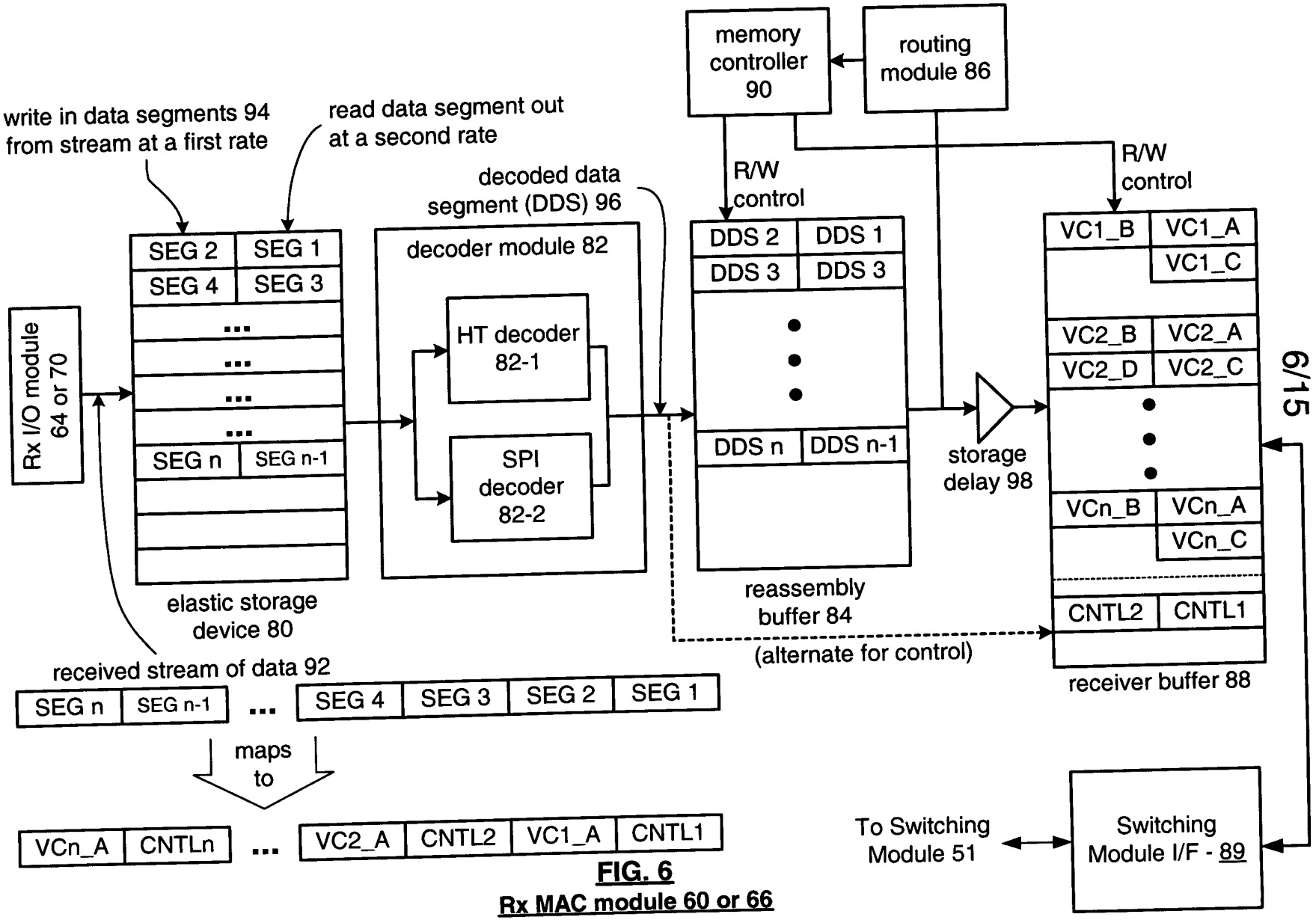


FIG. 6

Rx MAC module 60 or 66

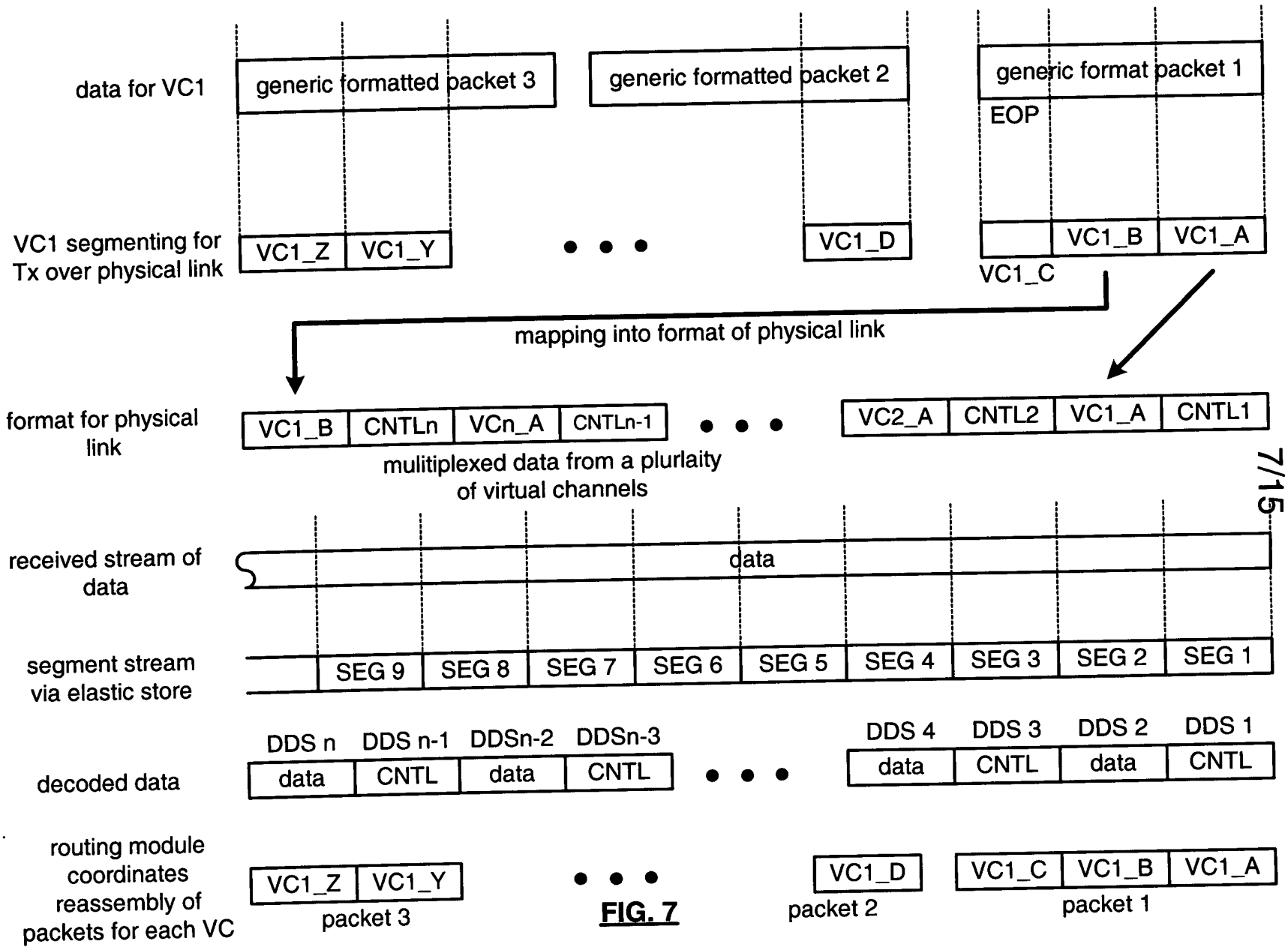

data for VC1
generic formatted packet 3
generic formatted packet 2
generic format packet 1
EOP
VC1 segmenting for Tx over physical link
VC1_Z
VC1_Y
VC1_D
VC1_C
VC1_B
VC1_A
mapping into format of physical link
format for physical link
VC1_B
CNTLn
VCn_A
CNTLn-1
VC2_A
CNTL2
VC1_A
CNTL1
mulitiplexed data from a plurlaity of virtual channels
7/15
received stream of data
data
segment stream via elastic store
SEG 9
SEG 8
SEG 7
SEG 6
SEG 5
SEG 4
SEG 3
SEG 2
SEG 1
DDS n
DDS n-1
DDSn-2
DDSn-3
DDS 4
DDS 3
DDS 2
DDS 1
decoded data
data
CNTL
data
CNTL
routing module coordinates reassembly of packets for each VC
packet 3
packet 2
packet 1

FIG. 7

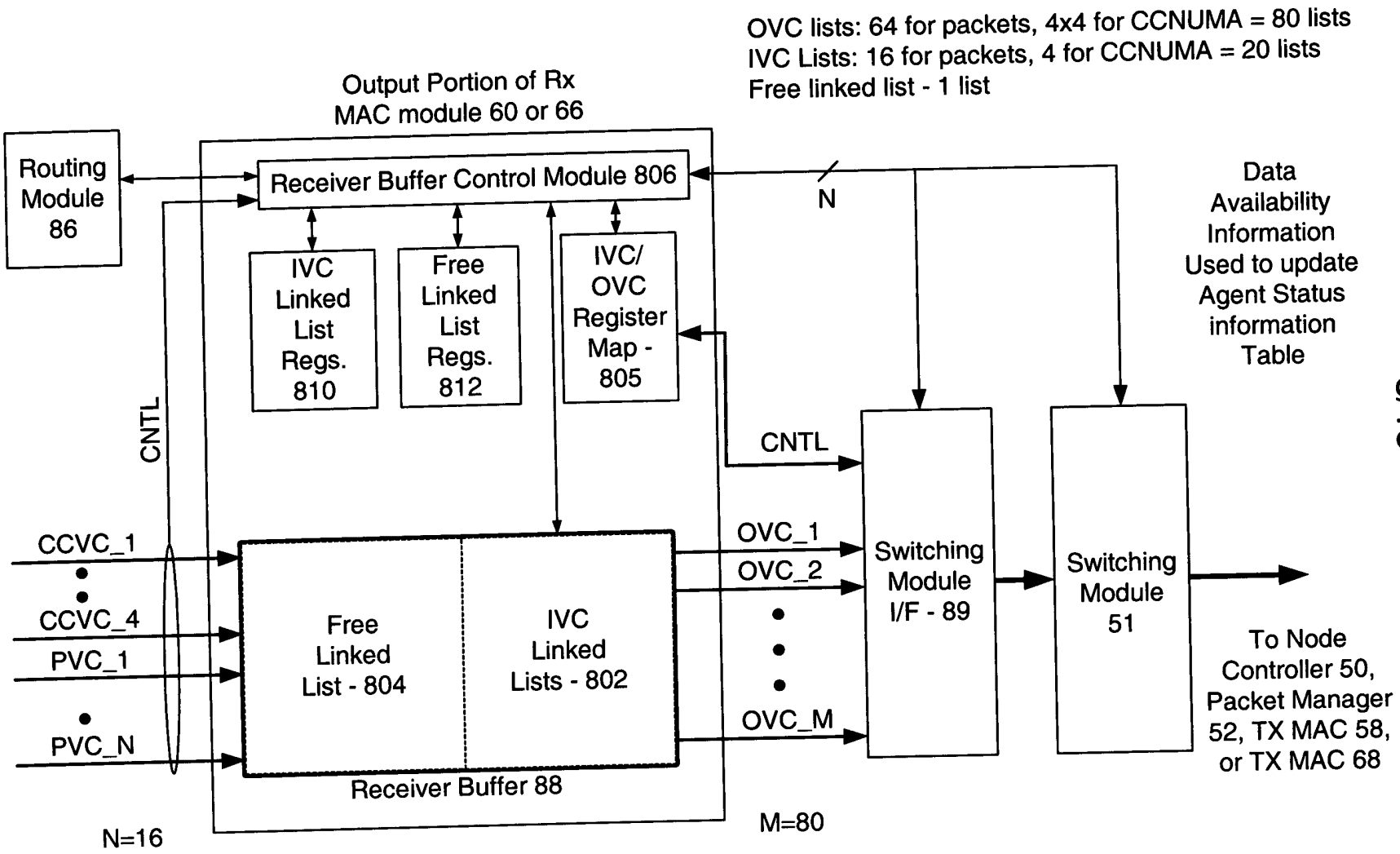

OVC lists: 64 for packets, 4x4 for CCNUMA = 80 lists
IVC Lists: 16 for packets, 4 for CCNUMA = 20 lists
Free linked list - 1 list
Output Portion of Rx
MAC module 60 or 66
Routing Module 86
Receiver Buffer Control Module 806
N
Data Availability Information Used to update Agent Status information Table
IVC Linked List Regs. 810
Free Linked List Regs. 812
IVC/ OVC Register Map - 805
CNTL
CNTL
CCVC_1
CCVC_4
PVC_1
PVC_N
Free Linked List - 804
IVC Linked Lists - 802
OVC_1
OVC_2
OVC_M
Switching Module I/F - 89
Switching Module 51
To Node Controller 50, Packet Manager 52, TX MAC 58, or TX MAC 68
Receiver Buffer 88
N=16
M=80

FIG. 8

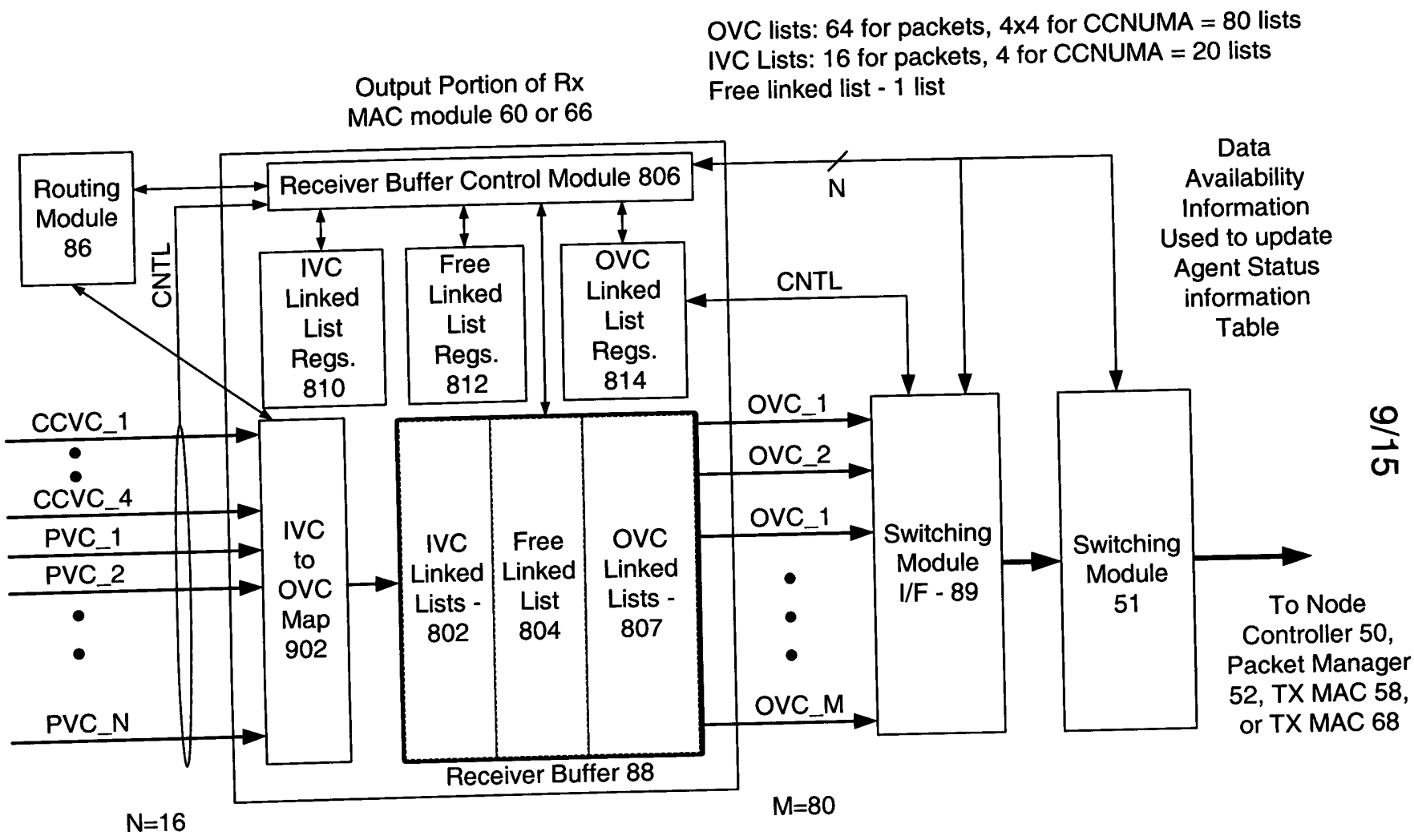

OVC lists: 64 for packets, 4x4 for CCNUMA = 80 lists
IVC Lists: 16 for packets, 4 for CCNUMA = 20 lists
Free linked list - 1 list
Output Portion of Rx
MAC module 60 or 66
Routing Module 86
Receiver Buffer Control Module 806
CNTL
IVC Linked List Regs. 810
Free Linked List Regs. 812
OVC Linked List Regs. 814
N
CNTL
Data Availability Information Used to update Agent Status information Table
CCVC_1
CCVC_4
PVC_1
PVC_2
PVC_N
IVC to OVC Map 902
IVC Linked Lists - 802
Free Linked List 804
OVC Linked Lists - 807
Receiver Buffer 88
OVC_1
OVC_2
OVC_1
OVC_M
Switching Module I/F - 89
Switching Module 51
To Node Controller 50, Packet Manager 52, TX MAC 58, or TX MAC 68
N=16
M=80

FIG. 9

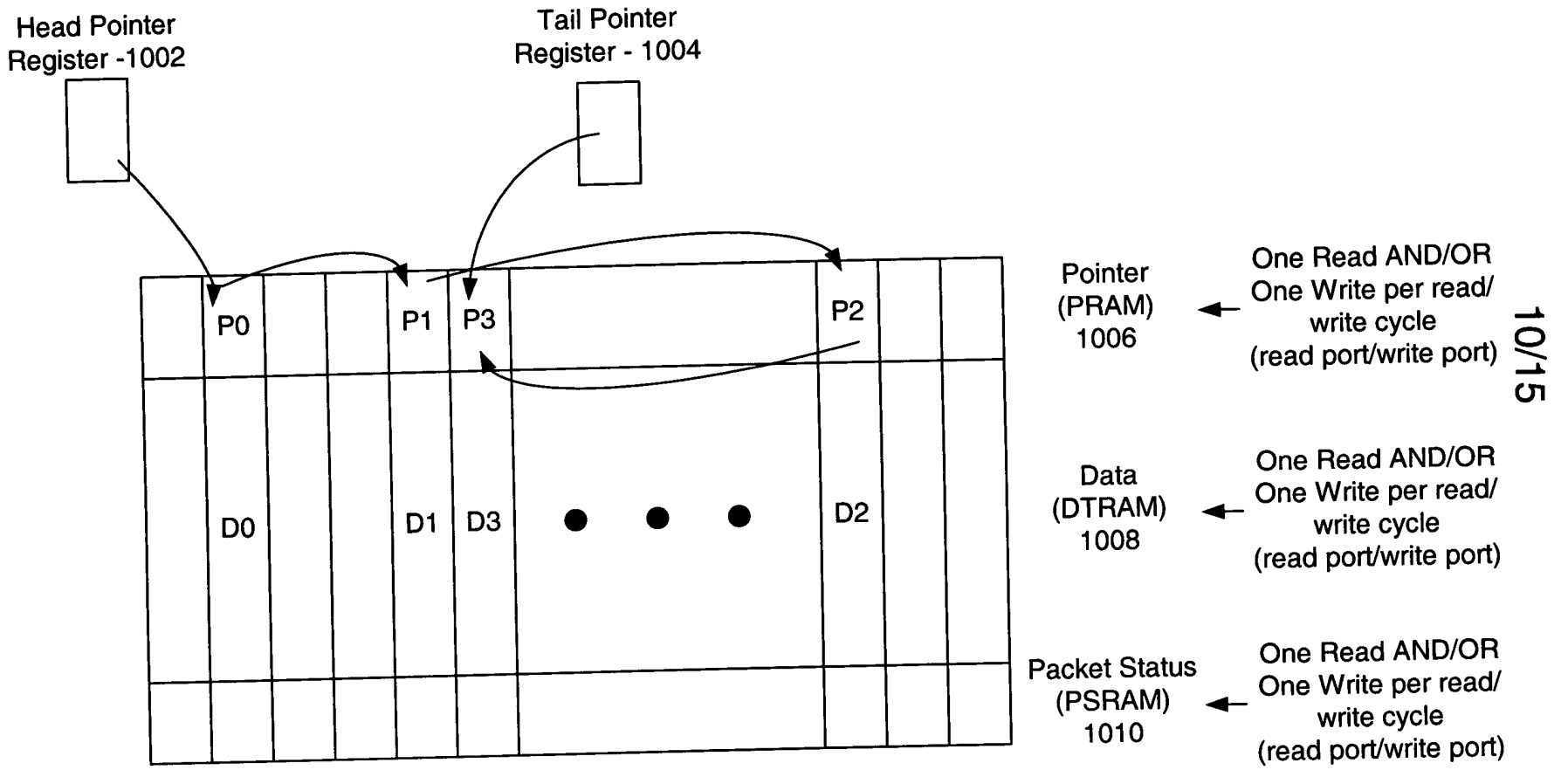

Head Pointer
Register -1002
Tail Pointer
Register - 1004
P0
P1
P3
P2
D0
D1
D3
D2
Pointer
(PRAM)
1006
One Read AND/OR
One Write per read/
write cycle
(read port/write port)
Data
(DTRAM)
1008
One Read AND/OR
One Write per read/
write cycle
(read port/write port)
Packet Status
(PSRAM)
1010
One Read AND/OR
One Write per read/
write cycle
(read port/write port)

FIG. 10

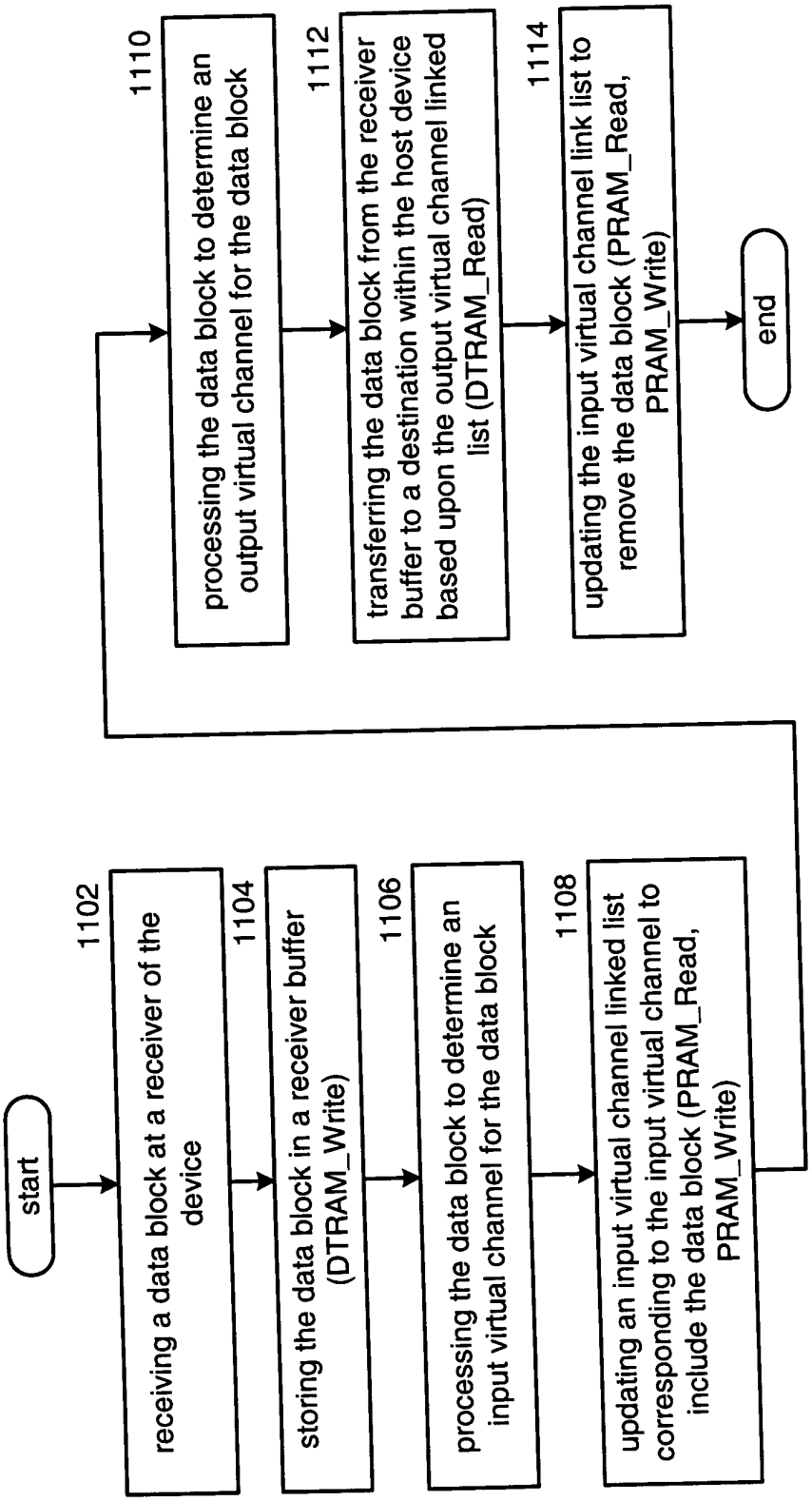

start
1102
receiving a data block at a receiver of the device
1104
storing the data block in a receiver buffer (DTRAM_Write)
1106
processing the data block to determine an input virtual channel for the data block
1108
updating an input virtual channel linked list corresponding to the input virtual channel to include the data block (PRAM_Read, PRAM_Write)
1110
processing the data block to determine an output virtual channel for the data block
1112
transferring the data block from the receiver buffer to a destination within the host device based upon the output virtual channel linked list (DTRAM_Read)
1114
updating the input virtual channel link list to remove the data block (PRAM_Read, PRAM_Write)
end

FIG. 11

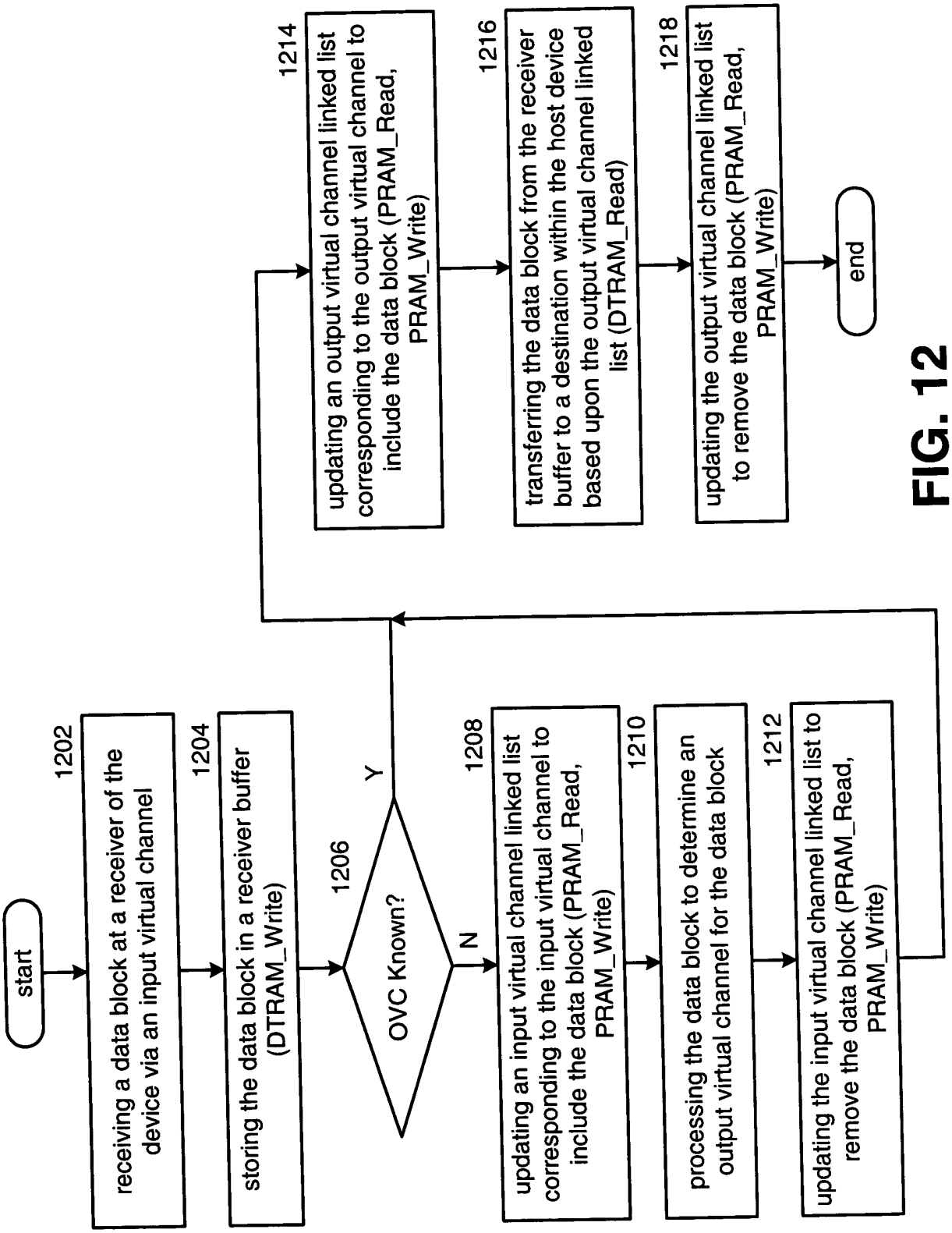

start
1202
receiving a data block at a receiver of the device via an input virtual channel
1204
storing the data block in a receiver buffer (DTRAM_Write)
1206
OVC Known?
Y
N
1208
updating an input virtual channel linked list corresponding to the input virtual channel to include the data block (PRAM_Read, PRAM_Write)
1210
processing the data block to determine an output virtual channel for the data block
1212
updating the input virtual channel linked list to remove the data block (PRAM_Read, PRAM_Write)
1214
updating an output virtual channel linked list corresponding to the output virtual channel to include the data block (PRAM_Read, PRAM_Write)
1216
transferring the data block from the receiver buffer to a destination within the host device based upon the output virtual channel linked list (DTRAM_Read)
1218
updating the output virtual channel linked list to remove the data block (PRAM_Read, PRAM_Write)
end

FIG. 12

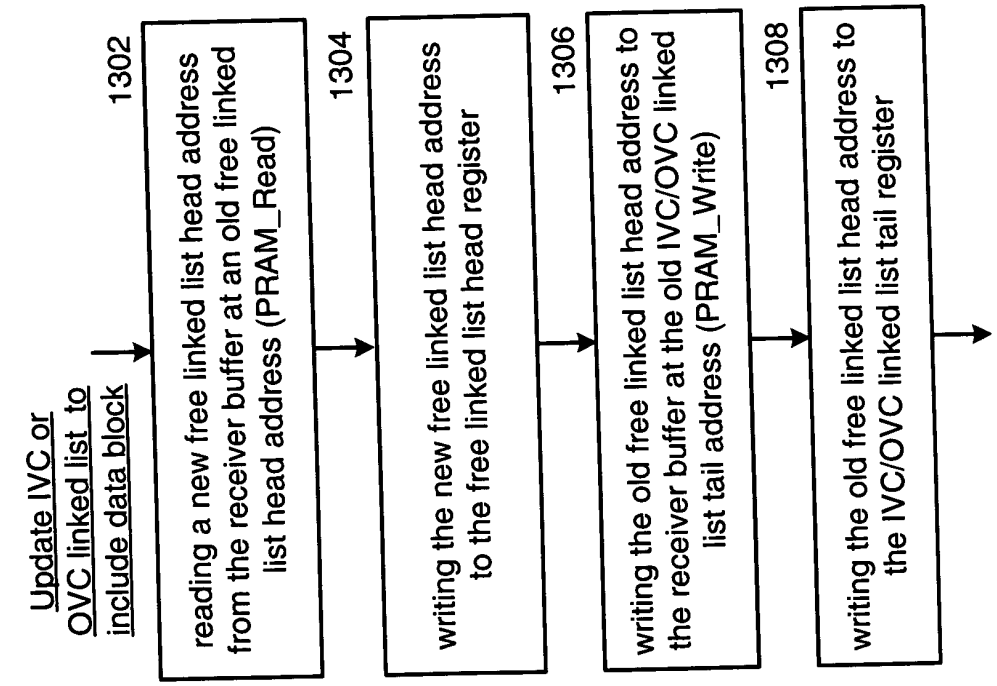


FIG. 13A

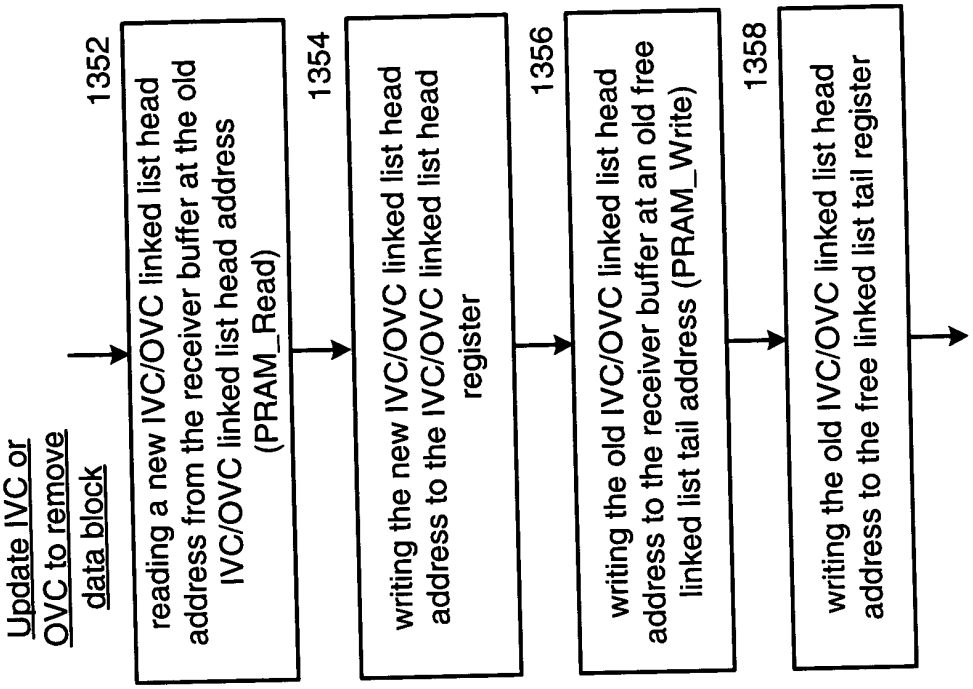


FIG. 13B

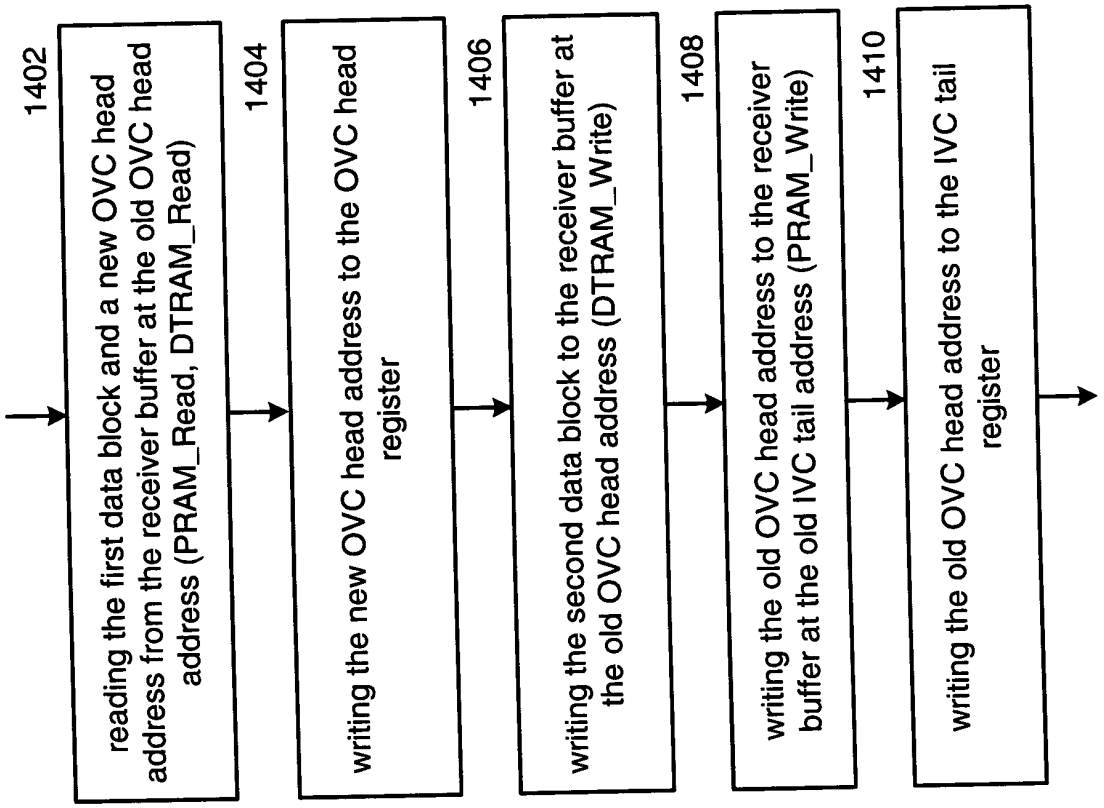
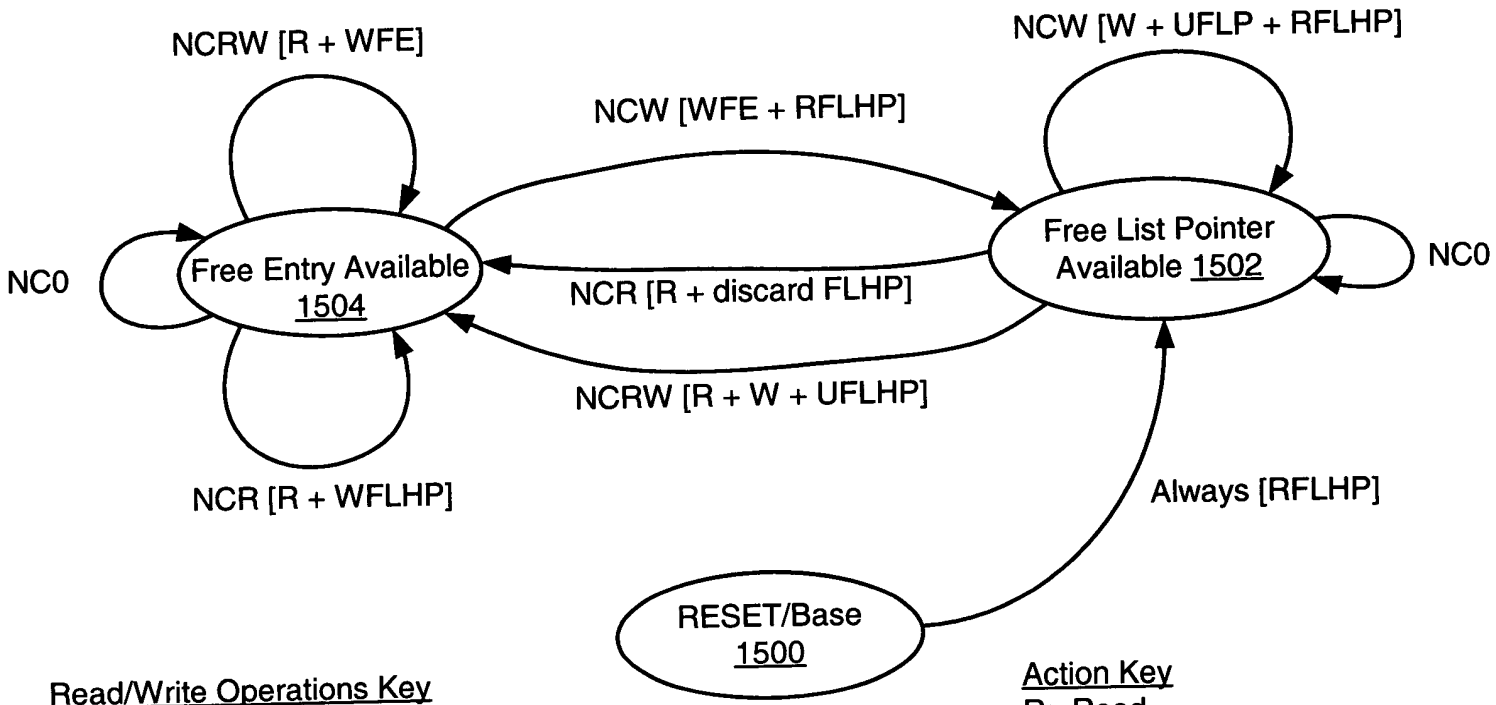

Read from OVC and Write to IVC in a single read/write cycle
1402
reading the first data block and a new OVC head address from the receiver buffer at the old OVC head address (PRAM_Read, DTRAM_Read)
1404
writing the new OVC head address to the OVC head register
1406
writing the second data block to the receiver buffer at the old OVC head address (DTRAM_Write)
1408
writing the old OVC head address to the receiver buffer at the old IVC tail address (PRAM_Write)
1410
writing the old OVC head address to the IVC tail register

FIG. 14



Read/Write Operations Key
NCR: Next Cycle Read
NCW: Next Cycle Write
NCRW: Next Cycle Read & Write
NC0: No reads/writes next cycle

Action Key
R: Read
W: Write
RFLHP: Read Free List Head Pointer
UFLHP: Update Free List Head Pointer
WFLHP: Write Free List Head Pointer
WFE: Write previously freed entry, no FL change

FIG. 15